**ICECS 2012 Tutorial Proposal**

**Format -** Half Day

Title**:**

# Using Logical Effort for Designing Carbon Nanotube FET (CNFET)-based Digital Circuits

Proposers/Authors

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**Areas**: Nanotechnology, Digital VLSI Design, Alternatives to CMOS, Logical Effort.

**Abstract:** Carbon Nanotube Field Effect Transistor (CNFET) is one of the most promising candidates for a building block of post silicon era integrated circuits because of its excellent electronic properties. Furthermore, ambipolar properties of carbon-nanotubes allow building compact generalized logic gates, based on XOR operations, and realizing many functions with fewer physical resources. CNT-based technology, however, is facing some major challenges; (1) variation in the diameter and density of the tubes that results in variation in delay and power consumption of CNT-based circuits, (2) the misalignment of CNTs that can result in incorrect logic functionality, (3) the presence of unwanted metallic carbon nanotubes, (4) the presence of Schottky barriers between the metal electrodes and the CNTs. This tutorial starts with a discussion on carbon nanotubes' electrical properties, possible CNFETs and simple gate configurations, and their performance, power and yield evaluation. A comparison with nano CMOS circuits will be presented as well. We will discuss technology challenges and current methods to dill with these challenges. One of the major challenges faced by the CNFET is the presence of unwanted metallic tubes that adversely impacts the delay, power and functional yield of CNT-based circuits. We will discuss CNFET-based circuit delay, power and yield in the presence variations of physical parameters of carbon nanotubes arrays, and variations due to removal of unwanted metallic tube. Monte Carlo simulations and results from newly developed analytical models are used to evaluate tradeoff between performance parameters and proposed gate- and circuit–level techniques to build robust circuits. Current technology,

device, circuit and layout methods, to reduce impact of other challenges will be presented and future technology and research directions will be proposed and discussed. Logical Effort for basic CNFET logic gates will be derived, discussed, and used for performance and yield evaluation. We will present methods to evaluate performance and yield of CNFET-based circuits in the presence of variations and the initial presence of metallic tubes. Comparison between CMOS and CNFET-based circuits will be presented using logical effort.

**Keywords**: Logical Effort, Carbon Nanotube (CNT), Carbon Nanotube Field Effect Transistor (CNFET), CNFET –based logic gates, functional yield, unwanted metallic tubes, tube misalignments, layout, Monte Carlo (MC) simulation, nano-architecture.

**Learning Objectives**: Present the current state-of-the-art technology for carbon nanotube FET-based digital circuits. Discuss main challenges, and introduce possible technology, layout, circuit and architecture solutions and their tradeoff. Introduce Logical effort as a tool for performance and yield comparison. Discuss future research directions and evaluate which are the most promising improvements paths.

**Target audience:** Electrical engineers with basic understanding of digital circuit design and its challenges due to scaling. Attendees with experience in digital circuit design and those with experience in nanotechnology will appreciate comprehensive presentation on relations between technology solutions and limitations and gate/circuit/architecture level techniques

**Prerequisites:** None. This is an introductory tutorial that can be easily understood by electrical and electronic engineers. The tutorial starts with introducing advantages of carbon nano tubes and current technologies to build carbon nanotube FET-based simple logic circuits. Challenges with current fabrication technologies are presented and evaluation of technological, circuit and layout methods are presented and discussed. The presentation focuses on understanding basic issues and evaluating possible solutions. All attempt are made to explain with graph, pictures and specific messages that are derived from experiments, analysis and simulations.

**Tutorial Description:**

Silicon based integrated circuit technology has witnessed aggressive scaling over the

last four decades but now it is approaching its physical limits. For sub-10nm technology node some of the devices that are under investigation by researchers are Si nanowire FETs, carbon nanotube field effect transistors (CNFETs), and III-V compound semiconductor quantum-well FETs. CNFETs are at the forefront of these devices because of its excellent electronic properties. The properties like near ballistic transport, high, in the range of $10^3$~$10^4 cm^2/Vs$, carrier mobilities in semiconducting CNTs, and easy integration of high-k dielectric material resulting in better gate electrostatics. Single-wall CNTs are hollow cylinders with a diameter in the range of 1-2nm. Two main types of CNFETs are being explored by researchers. These are the Schottky Barrier (SB) CNFETs and enhancement type CNFETs. The unipolar conduction characteristic and the absence of SB in enhancement type of CNFETs results in much lower *OFF* state leakage current and higher *ON* state current as compared to SB CNFET. Also, the enhancement-type of CNFETs are compatible with the current CMOS technology. Physical implementations of inverters, 5-stage ring oscillator, NAND, NOR gates, and SRAM cells build with CNFETs have been demonstrated.

For 32-nm technology node CNFETs have a potential for superior performance than their silicon counterparts. Under ideal conditions CNFETs are reported to be thirteen times faster than a PMOS transistor and six times faster than an NMOS transistor for a similar length of a channel. Single-tube CNFET's are not very feasible for circuit applications because of their low drive currents and small active areas. Scalable devices require the array of densely packed CNTs which will result in multiple parallel transport paths and hence can deliver large drive currents. Present synthesis technology allows us to pack almost 10-50 CNTs/mm. However to obtain delay and energy gains over Si-CMOS with future technology nodes almost 250 CNTs/mm are required.

There are some major challenges associated with the fabrication of CNFETs like variation in the diameter of tubes, unwanted growth of metallic tubes, and misaligned carbon nanotubes. The variation in the diameter of the tubes can result in variation in the drain current of CNFETs, however these variations can be averaged out due to statistical averaging of currents in multiple tube/channel transistors. Although fabricated CNTs are well aligned but a small percentage of CNTs still end up being misaligned. The presence of misaligned tubes and unwanted growth of metallic tubes poses a serious challenge in the building of reliable carbon nanotube based integrated circuits. The misalignment of tubes can result in incorrect functionality of logic gates. Recently, a new technique based on a proper layout design which allow for selective etching of misaligned tubes to make designed circuits function correctly even in the initial presence of misaligned tubes has been proposed. Similarly, the presence of metallic tubes creates a short circuit between the drain and source of a CNFET, which severely degrades the performance and

noise margin of carbon nanotube based gates and also results in large static power consumption. Current CNT synthesis techniques result between 4% to 40% metallic tubes.

Techniques such as current-induced electrical burning or selective chemical etching can be used to remove the metallic tubes. There are, however, additional issues related to tube removal techniques. To electrically breakdown a metallic nanotube the electrical burning technique requires a contact with each individual nanotube that is not easily scalable for ultra large-scale VLSI systems. On the other hand, chemical etching is scalable but since tube removal is based on cutoff tube diameter it may result in not completely removing the metallic tubes and also in removing some of the semiconducting tubes.

In this Tutorial we will focus on layout and circuit techniques to design robust CNFET-based digital circuits in the presence of fabrication challenges, variations, tube misalignment and metallic tubes. We will discuss yield-aware circuit techniques using different CNFET transistor configurations and tube-level, gate-level and circuit-level redundancy. Monte Carlo simulation results will be presented and discussed as a vehicle for further improvements. Metallic tube removal techniques and variations these techniques introduce will be discussed and circuit methods for their reduction will be introduced. Methods to improve a functional yield under performance and power constraints will be presented. We explore value of the logical effort technique to design robust CNFET-based circuits that due to the presence of unwanted metallic tubes and variations of device parameters behave as stochastic systems. We Will present capacitance-based logical effort models to estimate the delay of CNFET-based circuits in the presence of metallic tubes, and when the metallic tubes are removed by one of known processing techniques. Monte Carle simulation that uses the developed logical effort models to evaluate delay and functional yield of various types of stochastic logic gates and bigger building blocks will be presented and discussed. The impact of gate fanouts on simulations for fanout of one (FO1) and fanout of four (FO4) for inverter chain, NAND gate, and 4-stage decoder circuit will be shown. Potntial of the logical effort technique being very efficient in evaluation and optimization of stochastic CNFET-based designs is discussed. Future interesting research topics and most promising technology directions will be discussed.

<u>Papers written jointly by the Tutorial proposers, and directly related to the proposed Tutorial</u>


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Presenter's Bios**:**

**Malgorzata Chrzanowka-Jeske**

**Malgorzata Chrzanowska-Jeske** received her M.S. degree in electronics engineering from Politechnika Warszawska (the Technical University of Warsaw) in Warsaw, Poland, and the Ph.D degree in electrical engineering from Auburn University, Auburn, Alabama.

She has served on the faculty of the Technical University of Warsaw, and as a design automation specialist at the Research and Production Center of Semiconductor Devices in Warsaw. Since 1989, she is with the Department of Electrical and Computer Engineering at Portland State University in Portland, Oregon, currently as Professor and Chair of the department. Her research interests include CAD for VLSI IC, MS-SOC, 3D ICs, nanotechnology and nano/bio system, design for manufacturability and design issues in emerging and renewable technologies. She has published more than 100 technical papers and serves as a panelist for the National Science Foundation (NSF) and as a reviewer for National Research Council Canada (NRC) and many international journals and conferences.

Dr. Chrzanowska-Jeske has served on the Technical, Steering, and Organizing Committees of many international conferences, and was a Technical Chair of the 2002 International Conference on Electronics, Circuits and Systems. In 2004, she was a Guest Editor of the International Journal on Analog Integrated Circuits and Signal Processing. She is on the Board of Governors of IEEE Circuits and Systems Society and a Chair of DLP program. She is a member of the VLSI Systems and Applications and Nanoelectronics and Gigascale Systems Technical Committees of the IEEE Circuits and Systems Society, and a member of IEEE Council on Electronic Design Automation. She received the Best Paper Award from Alabama Section of IEEE for the best IEEE Transaction paper in 1990 and IEEE Council on Electronic Design Automation 2008 Donald O. Pederson Best Paper Award in IEEE Transactions on Computer-Aided-Design of Integrated Circuits and Systems.